Amendments to the Specification:

Please amend the paragraph labeled [0010] with the following amended paragraph:

[001] Referring now to FIG. 1, a circuit 10 is shown for determining the operating temperature of an active semiconductor device, here a transistor 12. The circuit 10 is located on a semiconductor substrate 14 (FIGS. 2A, 2B and 2C) having thereon the active device 12. Here the transistor 12 is a field effect transistor having source electrode, S, drain electrode D and gate electrode G, as shown.

Please amend the paragraph labeled [0015] with the following amended paragraph:

[002] The circuit 10 includes a tuning circuit 22 coupled to an output electrode of the transistor 12. The tuning circuit ~~12~~ 22 has a tunable element 24, here a varactor, controlled by a control signal fed to such tunable element 24 by a processor 26.

Please amend the paragraph labeled [0017] with the following amended paragraph:

[003] The processor 26 is responsive to the voltage produced at the output of the bridge 16 and a signal representative of power fed to the transistor 12. Any one of a variety of means may measure the power fed to the transistor 12, here, for example, such power is measured by a voltage V produced across a precision resistor R in the source circuit of the transistor 12. The voltage across this resistor is IR while the bias power into the transistor is this current multiplied by the voltage drop across the transistor.

Please amend the paragraph labeled [0019] with the following amended paragraph:

[004] More particularly, the process of self-alignment and dynamic tuning can be understood based on the following balance equation:

$P_{rf.load} + \sout{P_{rf,.tunrers}} \underline{P_{rf,.tunrer}} = P_{dc} - P_{diss} + P_{rf.in}$

where $P_{rf.load}$ is the power to the load, here represented in FIG, 1 by resistor Rl;

$\sout{P_{rf,.tunrers}}$ $\underline{P_{rf,.tunrer}}$ is the power dissipated in the tuner 22;

P_{dc} is the power fed to the transistor 12;

P_{diss} is the power dissipated in the transistor as represented by the output voltage of the bridge 16 (i.e., the voltage between nodes N1 and N3); and

$P_{rf.in}$ in the input radio frequency (rf)power fed to the gate G of transistor 12.